What is claimed is:

1. A pipelined adaptive decision feedback equalizer for equalizing a signal received from a channel, comprising:

a pre-processing unit (PP) comprising a plurality of PP coefficients for filtering the signal, and generating a PP output signal;

an adder receiving the PP output signal and outputting an added signal;

a slicer coupled to the output terminal of the adder, the slicer outputting a decision signal based on the added signal;

a feedback filter (FBF) comprising a plurality of FBF coefficients, coupled to the slicer for receiving the decision signal, the feedback filter canceling post-cursor ISI and generating a FBF output signal;

a delay unit coupled between the feedback filter and the second input terminal of the adder, the delay unit receiving the FBF output signal and generating the delayed FBF output signal to the adder, wherein the delay unit is a n_1-tap delay block, n_1 is positive integer and $n_1 \geq 2$;

a weight-update block for adapting the FBF coefficients to cancel the post-cursor ISI and selecting a plurality of FFF coefficients from the FBF coefficients; and

a mapping circuit for translating the FBF coefficients by a predetermined method to generate the PP coefficients and outputting the PP coefficients

to the pre-processing unit, wherein at least one element of the set of the FBF coefficients is different from the corresponding element of the set of the PP coefficients.

2. The pipelined adaptive decision feedback equalizer of claim 1, wherein the first weight-update block adapts the coefficients according to a Delay Least-Mean-Square algorithm.

3. The pipelined adaptive decision feedback equalizer of claim 1 further comprises:

a feedforward filter comprising a plurality of FFF coefficients, coupled between the pre-processing unit and the first input terminal of the adder, the feedforward filter canceling pre-cursor intersymbol interference (ISI) from the PP output signal and generating a FFF output signal to the adder;

a second weight-update block for adapting the FFF coefficients to cancel the pre-cursor ISI.

4. The pipelined adaptive decision feedback equalizer of claim 3, wherein the second weight-update block adapts the coefficients according to a Delay Least-Mean-Square algorithm.

5. The pipelined adaptive decision feedback equalizer of claim 1, wherein, in the mapping circuit, a relation between the third coefficient a_i and the first coefficient b_j is

$$(1-\sum_{i=1}^{M} a_i x^i)(1+\sum_{j=1}^{N} b_j x^j) = 1+\sum_{k=1}^{M+N} c_k x^k, \exists c_k = 0 \text{ if } 0<k<n_1;$$

wherein M is the number of the third coefficient, N is the number of the first coefficient and M, N, i, j and k are positive integers.

6. A decision feedback equalizer for equalizing a signal received from a channel, comprising:

a pre-processing unit (PP) comprising n_1 PP coefficients and a first delay unit, the pre-processing unit filtering the signal, and generating a PP output signal, wherein the first delay unit is a n_1-tap delay block, n_1 is positive integer and $n_1 \geq 2$;

a feedforward filter (FFF) comprising a plurality of FFF coefficients, coupled to the pre-processing unit to receive the PP output signal, the feedforward filter canceling pre-cursor intersymbol interference (ISI) and outputting a FFF output signal;

an adder having a first input terminal, a second input terminal and an output terminal, the first input terminal coupled to the feedforward filter, the output terminal outputting an added signal;

a slicer coupled to the output terminal of the adder, the slicer outputting a decision signal based on the added signal;

a feedback filter (FBF) comprising n_2 FBF coefficients and a third delay unit, coupled to the slicer, the feedback filter canceling post-cursor ISI and

outputting a FBF output signal, wherein the third delay unit is a n_3-tap delay block, n_2 and n_3 are positive integers and $n_2=n_3+n_1$;

a delay unit coupled between the feedback filter and the second input terminal of the adder, the delay unit receiving the FBF output signal and generating a delayed FBF output signal to the second input terminal of the adder, wherein the delay unit is a n_1-tap delay block;

a weight-update block for adapting the FBF coefficients to cancel the post-cursor ISI and selecting n_4 FFF coefficients from the FBF coefficients, wherein n_4 is the natural number and $n_4 \geq n_1$; and

a mapping circuit for translating the FBF coefficients by a predetermined method to generate the PP coefficients and outputting the PP coefficients to the pre-processing unit, wherein at least one element of the set of the FBF coefficients is different from the corresponding element of the set of the PP coefficients.

7. The pipelined adaptive decision feedback equalizer of claim 6, wherein the first weight-update block adapts the coefficients according to a Delay Least-Mean-Square algorithm.

8. The pipelined adaptive decision feedback equalizer of claim 6 further comprises:

a second weight-update block for adapting the FFF coefficients to cancel the pre-cursor ISI.

9. The pipelined adaptive decision feedback equalizer of claim 8, wherein the second weight-update block adapts the coefficients according to a Delay Least-Mean-Square algorithm.

10. The pipelined adaptive decision feedback equalizer of claim 6, wherein, in the mapping circuit, a relation between the fourth coefficient a_i and the first coefficient b_j is

$$(1-\sum_{i=1}^{M} a_i x^i)(1+\sum_{j=1}^{N} b_j x^j) = 1+\sum_{k=1}^{M+N} c_k x^k, \exists c_k = 0 \text{ if } 0<k<n_1;$$

wherein M is the number of the fourth coefficient, N is the number of the first coefficient and M, N, i, j and k are positive integers.